R is connected to reference signal $P_2(t)$ whose phase is θ_2. The difference between the phase θ_1 of feedback signal $P_1(t)$ and phase θ_2 of reference signal $P_2(t)$ is the phase error θ_e ($\theta_e = \theta_1 - \theta_2$). Phase error θ_e will cause up-down counter 22 to increase or decrease proportional to $\theta_e / 2\pi$, the count of which is utilized to alter output voltage V_o, which is proportional to θ_e as shown in Fig. 5. V_o increases if θ_e indicates a phase lag, causing an increase in the rate of pulses sent to motor 50 in order to increase the speed of motor 50. Conversely, V_o decreases if θ_e indicates a phase lead, causing a decrease in the rate of pulses sent to motor 50 in order to decrease the speed of motor 50.

In contrast, claim 1 recites in part:

> generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;
>
> providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;
>
> comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;
>
> generating a control signal based upon said comparison.

(Emphasis added) Applicants submit that such an invention is neither taught, disclosed nor suggested by Hsieh or any of the other cited references, alone or in combination, and includes distinct advantages thereover.

Hsieh teaches the use of the comparison of the phase of a signal generated by a speed detector to the phase of a reference signal, to adjust the input to a motor. Hsieh compares the phase of a reference signal to the phase of a feed back signal, and uses the difference thereof to create a phase error signal θ_e. Hsieh's invention strives to reduce the phase error signal by altering

the driving signal to motor 50, thereby altering the speed of motor 50. The phase error θ_e causes up-down counter 22 to increase or decrease, depending on whether the phase error θ_e is positive or negative. The output of up-down counter 22 is converted to an analog signal, referred to as a pump voltage, which is used to increase or decrease the rate at which pulses are sent to motor 50. The change in the speed of motor 50 alters phase θ_1 of feedback signal $P_1(t)$. This change in phase θ_1 relative to phase θ_2 of reference signal $P_2(t)$ is continuously monitored and sampled to control the speed of motor 50. In contrast thereto, Applicants' invention provides a generated reference signal, a proportional error signal and an error direction signal from a signal having the desired frequency and an encoder output signal. Applicants' invention uses the generated proportional error signal and the error direction signal to control the speed of a target system. Unlike Hsieh, Applicants' invention does not depend on measuring phase differences of two signals and controlling the speed of a target system to minimize the phase differences thereof. Rather, Applicants' invention compares the frequency of two signals and minimizes the frequency difference thereof. As such, Hsieh fails to disclose or suggest generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal, providing a target system to be regulated, the target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency, comparing the frequency of the reference pulse train with the frequency of the feedback pulse train and generating a control signal based upon the comparison, as recited in claim 1.

The Examiner notes that the output of frequency divider 82 has a frequency output that is dependent on the frequency of the input. While that is the nature of a frequency divider, a frequency divider is not a part of the Applicants' invention. Further, the Examiner states broadly

that phase detector 10 compares pulse trains, but Hsieh teaches that phase detector 10, during each period T, compares the difference between phase θ_1 of feedback signal $P_1(t)$ with phase θ_2 of reference signal $P_2(t)$ and generates thereby a square pulse with the duration thereof in proportion to phase error θ_e (column 4, lines 12-17).

An advantage of the Applicants' invention is that less space is needed since less circuitry is used because phase detection of two signals, comparison of the relative phases of the two signals and the generation of a phase error correction signal are not necessary. Further, since phase differences are not detected and not corrected for in Applicants' invention, costs are reduced and the invention finds application in design scenarios where the cost of controlling speed by detecting phases of signals is prohibitive. Yet another advantage of Applicants' invention is that there is less noise in the control system than is present in phase detection and control circuits. Accordingly, Applicants submit that claim 1, and claim 8 depending therefrom, are now in condition for allowance, which is hereby respectfully requested.

Claims 2, 3 and 5 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,212,434 (Hsieh) in view of either U.S. Patent No. 4,494,509 (Long) or U.S. Patent No. 6,043,695 (O'Sullivan). However, claims 2, 3 and 5 depend from claim 1, which is in condition for allowance for the reasons given above. Accordingly, Applicants submit that claims 2, 3 and 5 are now in condition for allowance, which is hereby respectfully requested.

The Examiner has indicated that claims 4, 6 and 7 are allowed. For the courtesy thereof, the Applicants thank the Examiner.

For the foregoing reasons, Applicants submit that no combination of the cited references teaches, discloses or suggests the subject matter of the claims. The pending claims are therefore in

condition for allowance, and Applicants respectfully request withdrawal of all rejections and allowance of the claims.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (219) 897-3400.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on: September 25, 2001.

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September 25, 2001
Date